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Examiner: A. Chambliss
Art Unit: 2814

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : K. TATSUMI, et al.

Serial No.: 09/254,119

Filed : April 16, 1999

For : SEMICONDUCTOR DEVICE PROVIDED WITH LOW MELTING
POINT METAL BUMPS

Assistant Commissioner
for Patents
Washington, D.C. 20231

#12/
9-1501
Payton

RESPONSE

SIR:

Reconsideration of the above-identified patent application is respectfully requested. This communication is responsive to the Office Action mailed March 28, 2001. A petition for an extension of time in which to respond to the Office Action accompanies this response. A Notice of Appeal accompanies this response.

Claims 1-6 are pending in the application.

§103

Claims 1-3 were rejected under 35 U.S.C. §103(a) as being unpatentable over Japan No. 6-333930 to Atsuhiko in view of U.S. Patent No. 5,542,601 to Fallon et al.

Claims 4-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over Atsuhiko-Fallon and further in view of Japan No. 59-148352 to Hisao.

These rejections are respectfully traversed.

Claim 1 is the only pending independent claim.

Claims 2-6 depend from claim 1.

Applicants submit that neither Japan No. 6-333930 to Atsuhiko nor Japan No. 59-148352 to Hisao disclose or suggest the feature of the defined radius R of the metal balls set forth in independent claim 1.

The current Office Action cites for the first time U.S. Patent No. 5,542,601 to Fallon et al as disclosing the defined radius R of the metal balls. Applicants maintain that Fallon et al. do not disclose or suggest the defined radius R of the metal balls.

U.S. Patent 5,542,601 (Fallon et al.), which has been newly cited in the present Office Action in addition to the references cited in the last Office Action, relates to a process for removing defective semiconductor chips, mounted in a flip chip configuration, from an organic substrate, such as an organic printed circuit board (PCB) or printed circuit card (PCC). Fallon describes a rework process for a defective semiconductor chip attached to contact pads on an organic substrate via solder balls.

The technology of Fallon et al. is based on the fact that the conventional rework process used in connection with chips mounted on a PCB or PCC is undesirable where the chips have solder ball grid pitches smaller than 14 mils and/or where the dimensions of the contact pads on the corresponding PCB or PCC are smaller than 5 mils by 6 mils. Such conditions lead to undesirable solder bridging between adjacent solder balls and/or adjacent contact pads causing undesirable short circuits. The passage cited by the Office Action refers to an example of a solder ball grid pitch of 9 mils and a contact pad surface area of 15 square mils (3 mils by 5 mils).

The present invention provides a semiconductor device provided with bumps formed from a solder ball, wherein the radius R of the metal ball and a surface area A of an electrode on the chip, on which the solder ball is provided for the formation of the bump satisfy the equation: $0.4\sqrt{A} \leq R \leq 2\sqrt{A}$. The semiconductor device according to the present invention is free of fracture at the bonded portions between the bumps and the electrodes (see the specification, page 9, lines 31 to 35). Thus, the present invention makes it possible to mount a semiconductor device on a substrate by a flip chip bonding technique, with high reliability.

As is clear from the above, Fallon et al. refers to the requirement for preventing adjacent solder bumps (solder

balls) from being bridged therebetween during the removal of defective semiconductor chips, which have already been attached to a substrate such as a PCB, and replacement thereof with functional semiconductor chips, with the requirement involving a solder ball pitch and dimensions (or a surface area) of an electrode pad. In contrast, the present invention specifies the requirement for reliable bonding between bumps and electrodes, which involves the relation between the radius of the solder ball and the surface area of the electrode on a mounting substrate.

Thus, the requirement in the technology of Fallon et al. involves the solder ball pitch and not the size (radius) of the solder ball itself as in the present invention.

Further, the requirement in the present invention defines the relation between the solder ball radius R and the electrode surface area A to provide satisfactory solder bumps on the electrodes, to thereby make it possible to form good semispherical bumps on the electrodes after a reflowing process, the bump having much less tendency to be fractured due to stress concentration compared to those not satisfying the requirement. This effect of the present invention is neither disclosed nor suggested in Fallon et al. Consequently, no combinations of references cited in the

Office Action make the present invention obvious to a person with ordinary skill in the art.

In addition, it should be noted that the present invention specifies the upper and lower limits of solder ball radius R, whereas Fallon et al. merely describes a preselected amount of solder being determined empirically (column 6, lines 20 to 22), and neither discloses or suggests upper and lower limits as specified in the invention of the application. Incidentally, it should be also noted that, when $R = 9$ mils and $A = 15$ square mils, as indicated by the Office Action, the equation in the present invention is not satisfied.

$2\sqrt{15} = 2 \times 3.87 = 7.74$. If $R = 9$, 9 is not less than or equal to 7.74. Therefore, the equation set forth in independent claim 1 is not satisfied.

It is therefore submitted that independent claim 1, and claims 2-6 dependent thereon, are patentable over Atsuhiko, Hisao and Fallon et al. taken in any combination.

Priority Document

The status of the priority document is respectfully requested.

The present application claim convention priority under 35 U.S.C. §119 from Japanese Patent Application No. 8-244269 filed August 27, 1996. The Office Action mailed July 5, 2000 appears to indicate that the priority document has

not been received. The Office Action mailed March 28, 2001 does not address the priority document.

In divisional Application No. 09/632,910, an Office Action mailed August 14, 2001 indicates that all of the priority applications have been received and certified copies are received in Application No. 09/254,119 (the present application).

The status of priority patent application Japan No. 8-244269 is requested in the next communication from the Patent and Trademark Office.

CONCLUSION

It is submitted that in view of the foregoing remarks, the application is now in condition for allowance. It is therefore respectfully requested that the application, be allowed and passed for issue.

Respectfully submitted,

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